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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,269	12/12/2001	Andrew Cofler	S01022/80810	9647

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EXAMINER	
DILDINE JR, R STEPHEN	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,269	COFLER, ANDREW ET AL.	
	Examiner	Art Unit	
	R. Stephen Dildine	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,12,14,15 and 18* is/are rejected.

7)☐ Claim(s) *4-11, 13, and 16-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/12/2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/748,075.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/03 & 12/12/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

The drawings are objected to under 37 CFR 1.83(a) because they fail to show Figure 8 as described in the specification at page 10. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The specification is objected to because of the following informalities: page 10, "81" should be – 101 --. Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 09/748,077 in view of Roth et al. (2002/0078329, cited by applicant). A comparison of claims 1-3 with these references follows:

This Application		09/748,077		Roth et al.	
Claim 1	Guard indicators	Claim 1	"each instruction includes a guard"		
	instruction supply unit		"a fetch unit for fetching instructions to be executed"		
	pipelined execution unit		"at least one pipelined execution unit "		
	Emulator		"an emulation unit including control circuitry "		
	watch circuitry			Roth et al. Page 1, ¶ 12	"Generation of precise watchpoint matches for instructions and data facilitates debugging and enables code patching."
	Synchronising circuitry	Page 5, ¶ 62	"The timing of the synchronisation system 104 will be explained with reference to FIG. 12. The cycles of operation of instruction fetches, execution pipelines and memory accesses are controlled by clock cycles with a clock signal as shown at 230 in FIG. 7"		
Claim 2	watch circuitry is arranged for watching instruction fetch addresses			Roth et al. Page 1, ¶ 10	watchpoint engine 16 may be adapted to match on addresses of data or instructions,
Claim 3	emulator includes said watch circuitry			Roth et al. Page 1, ¶ 12	"The propagation of instructions through a processor pipeline can be monitored in real-time to identify emulation and exception events and provide emulation mode operation"

Clearly, it would be necessary and obvious to one of ordinary skill in the art at the time of applicants' invention to provide synchronizing circuitry in view of the statements at page 5, paragraph 62. Further, it would have been obvious to one of ordinary skill in the art at the time of applicants' invention to provide watch circuitry in the emulator in view of Roth et al.'s statement at paragraph 12, page 1 "Generation of precise watch point matches for instructions and data facilitates debugging and enables code patching".

This is a provisional obviousness-type double patenting rejection.

Claims 1-3, 12, 14 and 15 are provisionally rejected under the judicially created doctrine of double patenting over claim s 1, 6-8, 10, 12 and 15 of copending Application No. 09/748,762. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: a comparison of these claims with this references follows:

This Application		09/748,762	
Claim 1	Guard indicators	Claim 7	"each of said instructions includes a guard value "
	instruction supply unit	Claim 1	"said system including instruction fetch circuitry "
	pipelined execution unit	Claim 1	"dispatching fetched instructions to said pipelined execution unit"
	Emulator	Claim 10	"is effected by a emulator circuitry having "
	watch circuitry	Claim 12	"watch of the program count for use in debugging the data memory access operation by breaking the instruction sequence
	Synchronising circuitry	Claim 15	"which the data memory access operations are synchronised with respective program counts"
Claim 2	watch circuitry is arranged for watching instruction fetch addresses	Claim 12	"watch of the program count for use in debugging the data memory access operation
Claim 3	emulator includes said watch circuitry	Claim 12	"a emulator circuitry having diagnostic circuitry " (claim 10) " diagnostic circuitry operates to generate a
Claim 12	a plurality of execution units are provided in parallel and a plurality of instructions are dispatched simultaneously to respective execution pipelines	Claim 8	" plurality of parallel execution pipelines is provided"

This Application		09/748,762	
Claim 14	guard indicators	Claim 7	"each of said instructions includes a guard value "
	supplying a plurality of instructions to at least one pipelined	Claim 1	"instruction dispatch circuitry for dispatching fetched instructions to said pipelined execution unit"
	provide a commit signal if the instruction is executed	Claim 7	"commit indicators after resolution of the guard values of instructions fed to the execution pipeline to indicate whether execution of the instruction is committed"
	effecting a debugging watch	Claim 12	"watch of the program count for use in debugging the data memory access operation by breaking the instruction
	providing a program count signal	Claim 1	"in accordance with a program count"
	storing the program count in a sequential buffer	Claim 6	"buffers, each arranged to hold successive values of respective parameters in an order sequence, one of said parameters being successive program counts"
	storing in a further sequenced buffer commit signals derived from resolution of the	Claim 7	"each of said instructions includes a guard value and one of said buffers is arranged to hold commit indicators after resolution of the guard
Claim 15	a plurality of other parameters are watched by the debugging routine and detection of the parameters is stored in further	Claim 6	"in which the synchronising circuitry comprises a plurality of multivalue buffers, each arranged to hold successive values of respective parameters in an order sequence, one of said

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claims 1, 3, 12 and 18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 5, 8-9 of copending Application No. 09/748,785. Although the conflicting claims are not identical, they are not patentably distinct from each other. A comparison of claims 1, 3, 12 and 18 with the claims of copending Application No. 09/748,785 follows:

This Application		**09/748,785**	
Claim 1	Guard indicators	Claim 1	"guard register file holding values of the guards"
	instruction supply unit	Claim 1	"a fetch unit for fetching instructions to be executed"
	pipelined execution unit	Claim 1	"at least one pipelined execution unit "
	Emulator	Claim 1	"and an emulation unit including "
	watch circuitry	Claim 1	"to implement a precise watch or a non-precise watch "
	Synchronising circuitry	Parag. 45	
Claim 3	emulator includes said watch circuitry	Claim 5	"emulation unit is in a precise watch mode"
Claim 12	a plurality of execution units are provided in parallel and a plurality of instructions are dispatched simultaneously to respective execution pipelines	Claim 8	"which includes a plurality of parallel pipelined execution units, including at least two data unit pipelines for executing data processing instructions "
Claim 18	a plurality of instructions are supplied simultaneously to a plurality of parallel execution pipelines the resolution of guard values for each of the instructions being effected during passage through the execution pipeline	Claim 9	"at least one pipelined execution unit for executing decoded instructions and being associated with a guard register file holding values of the guards to allow resolution of the guards to be made" (claim 1) "according to claim 1, which includes a plurality of parallel pipelined execution units, including at least two data unit pipelines for executing data processing instructions and at least two address unit pipelines for executing memory access instructions" (claim 9)

The reference discloses (see paragraph 45 e.g.) that a synchronizing circuit is an obvious necessity in order to make the combination claimed in copending Application No. 09/748,785 operative.

Allowable Subject Matter

Claims 4-11, 13 and 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pardo (5,754,839) shows implementation of watch points in a data processing system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. Stephen Dildine whose telephone number is 703-305-5524. The examiner can normally be reached on M, Tu, Th, F 5:55 am to 4:25 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

R. Stephen Dildine
Primary Examiner
Art Unit 2133

R. Stephen Dildine
May 17, 2005